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Question Paper Code : 80121

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Fourth Semester

Electronics and Communication Engineering

EC 8452 — ELECTRONIC CIRCUITS — II

(Common to Electronics and Telecommunication Engineering)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Why frequency compensation is required in amplifiers?

2. What is gain margin?

3. Draw the electrical equivalent circuit of crystal.

4. What is the need for amplitude control in oscillators?

5. State the difference between loaded and unloaded Q.

6. What is the basic principle behind tuned amplifiers?

7. State the condition under which the RC high pass filter can act as a differentiator.

8. Why clamper circuit is called DC restorer?

9. Define the term Total Harmonic Distortion.

10. What is a DC/DC converter?

PART B — (5 × 13 = 65 marks)

11. (a) Discuss the effects of negative feedback on the properties of amplifiers in detail with relevant analytical expressions.

Or

(b) Discuss in detail about the impact of feedback on the amplifier with single and two poles.

12. (a) With relevant diagrams, explain the operation of (i) Ring oscillator and (ii) Crystal oscillator.

Or

(b) With a neat diagram, explain the operation of the Wien-bridge oscillator. Also derive the expression for the frequency of oscillation.

13. (a) Explain how flat band response is achieved in stagger tuned amplifier?

Or

(b) Discuss on the effect of cascading single and double tuned amplifier on bandwidth.

14. (a) With circuit diagram, waveforms and relevant expressions explain the operation of (i) Attenuator and (ii) RC integrator.

Or

(b) Explain with circuit diagram, waveforms and relevant expressions the operation of UJT oscillator.

15. (a) Explain the different classes of power amplifiers and compare them.

Or

(b) Explain the working of the three commonly used DC/DC converters with circuit and response diagrams.

PART C — (1 × 15 = 15 marks)

16. (a) Consider a three-pole amplifier with a loop gain function given by,

$$T(f) = \frac{10^5}{\left(1 + j\frac{f}{5\times10^5}\right)\left(1 + j\frac{f}{10^2}\right)\left(1 + j\frac{f}{5\times10^8}\right)}$$

Stabilize the circuit by inserting a new dominant pole. Assume the original poles are not altered. At what frequency must the new pole be placed to achieve a phase margin of 45 degrees?

Or

(b) An enhancement-mode MOSFET class-AB output stage is shown in the Fig.16(b). The threshold voltage of each transistor is $V_{TN} = -V_{TP} = 1v$ and the conduction parameters of the output transistors are $K_{n1} = K_{p2} = 5\ mA/V^2$. Let $I_{Bias} = 200\mu A$.

(i) Determine $K_{n3} = K_{p4}$ such that the quiescent drain currents in M_1 and M_2 are 5 mA. (6)

(ii) Find the small-signal voltage gain $A_v = d_{v0}/d_{v1}$ at $v_0 = 5v$. (9)